AUDIO BOARD — front end: power, U.FL audio in, reconstruction filter + buffers, 1/4in L/R + 3.5mm out

CTRL FFC -> break-off control board: SPI2 bus + 2 chip-selects (CS_CTRL, CS_CTRL2 from APM J7.7/J7.10) + 3V3/+5V/GND.
Control board digitizes its own pots/switches over SPI (ADC + shift-reg/mux): STM32 reads them and streams CVs to the DACs.

OUTPUTS — 1/4in L/R (ACJS-MHOM) + 3.5mm headphone/debug

FRONTEND
FILT_L_IND
FILT_L_IN
FILT_R_IND
FILT_R_IN
File: FRONTEND.kicad_sch

ANALOG_FILTER_CV
SPI_SCK
SPI_MOSI
CS_DAC1
MODE_SEL
FILT_L_IN
FILT_L_OUT
FILT_R_IN
FILT_R_OUT
CV_FX3
File: ANALOG_FILTER_CV.kicad_sch

+5V
PWR_FLAG
PWR_FLAG
GND

FX_RETURN_ADJUSTER
FX_RET_L
FX_RET_R
VOL_L
VOL_R
MF_CV_CUTOFF
MF_CV_RES
MF_MODE_A
MF_MODE_B
File: FX_RETURN_ADJUSTER.kicad_sch

H1 M2
H3 M2
H2 M2
H4 M2

POWER
File: POWER.kicad_sch

J9 U.FL FILT OUT
J10 U.FL FX send R
J11 U.FL FX return L
J12 U.FL FX return R
FILT_L_OUT
FILT_R_OUT
FX_RET_L
FX_RET_R
GND

R222 0
R223 0

ANALOG PATH — each channel's buffer output (FILT_x_IN) goes into the analog sub-sheet; FILT_x_OUT returns to the jacks

J4 1/4in L
J5 1/4in R
S1 S2 R1 RN1 T1 TN1
GND
LINE_L
LINE_R

J6 3.5mm HP
S R HP_R T HP_L GND

FX_RGND
FX_RGND
VOL_LGND
VOL_RGND

+5V
GND
MF_CV_CUTOFF
MF_CV_RES
GND
MF_MODE_A
MF_MODE_B
GND

FX_CONTROL
SPI_SCK
SPI_MOSI
CS_DAC2
CV_CUTOFFD
CV_RESD
MF_CV_CUTOFF
MF_CV_RES
File: FX_CONTROL.kicad_sch

SPI_SCK 1
SPI_MOSI 2
SPI_MISO 3
CS_DAC1 4
CS_POTS 5
MODE_SEL 6
GATE 7
8
9
CS_DAC2 10
J22 CTRL->FX FFC
GND

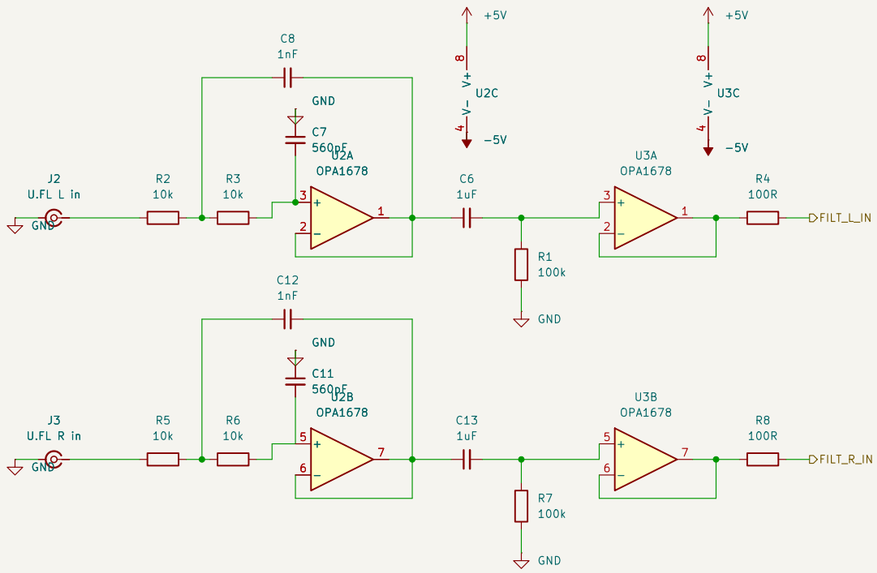
#PWR4022
#PWR4007
SPI_SCK 2
SPI_MOSI 3
SPI_MISO 4
CS_POTS 5
MF_MODE_A 6
MF_MODE_B 7
8
GATE 9
DETECT_PANEL
J8 CTRL->PANEL FFC

OUTPUT_BUF
VOL_L
VOL_R
LINE_L
LINE_R
HP_L
HP_R
File: OUTPUT_BUF.kicad_sch

MASTER VOLUME — RV4/RV5 = one dual-gang pot (shared L/R knob); attenuates final output to the jacks/HP

Sheet: /
File: AUDIO_BOARD.kicad_sch
Title:
Size: A2 | Date: | Rev:
KiCad E.D.A. 10.0.6 | Id: 1/9

AUDIO INPUT
– U.FL for L and R DACs from APM

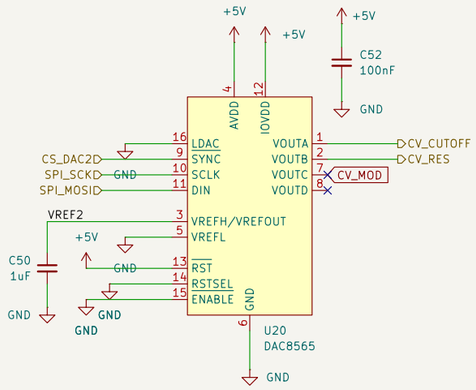


Sheet: /FRONTEND/		
File: FRONTEND.kicad_sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. 10.0.6		Id: 2/9

FX CONTROL – 2nd FX-control FFC (SPI + mode/order/enable) -> DAC8565 #2 makes CV_CUTOFF/CV_RES (+2 spare FX CVs); digital selects pass through

CONTROL/DAC – SPI + CS_DAC2 + CS_EXP from the root's one 10-pin control FFC; this DAC + the MCP expander share that SPI bus.

DAC decoupling



MCP23S17 expander – SPI2 + CS_EXP -> 16 GPIO fan-out for all FX/filter digital selects (frees the FFC from per-line GPIO). Runs at +3V3.

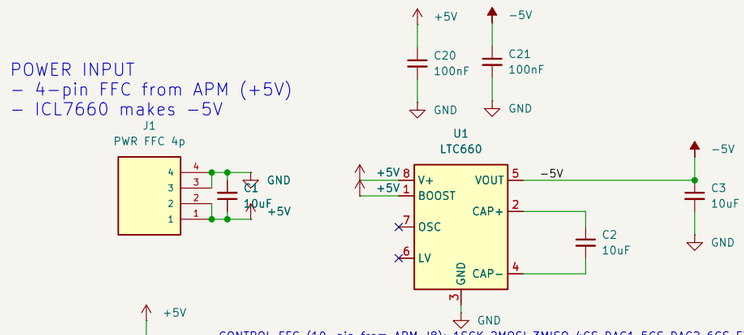
outputs to filter/FX: CV_CUTOFF, CV_RES (-> SVF), CV_FX1/CV_FX2 (-> future phaser/chorus/tremolo); MODE_A/B, ORDER_SEL, FX_EN1/2 digital.

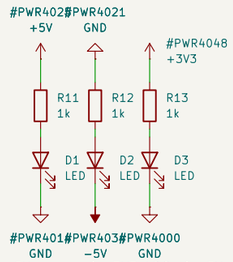
Knobs/switches live on the controller board; STM32 reads them, drives this DAC over SPI and sets the digital lines.

Sheet: /FX_CONTROL/		
File: FX_CONTROL.kicad_sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. 10.0.6		Id: 3/9

POWER FFC (4-pin from APM): +5V +3V3 GND GND (-5V made on-board)

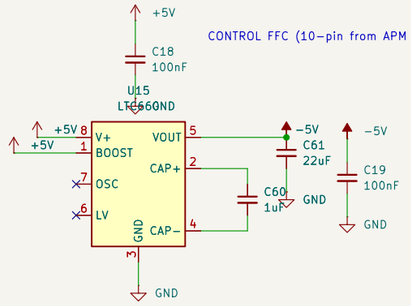
POWER INPUT
- 4-pin FFC from APM (+5V)
- ICL7660 makes -5V

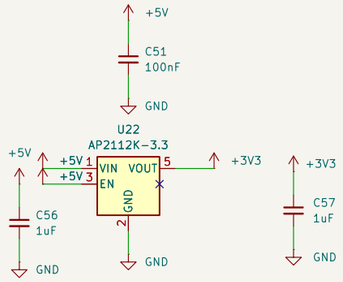




STATUS LEDs: +5V power / +3V3 LDO / -5V charge pumps

CONTROL FFC (10-pin from APM J8): 1SCK 2MOSI 3MISO 4CS_DAC1 5CS_DAC2 6CS_EXP 7sp 8/9GND 10sp





+3V3 LDO - AP2112K-3.3 from +5V (power FFC carries no +3V3); supplies only the MCP expander.

Sheet: /POWER/
File: POWER.kicad_sch

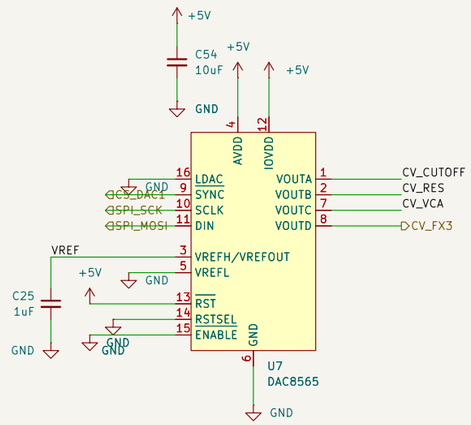
Title:

Size: A3 | Date: | **Rev:**

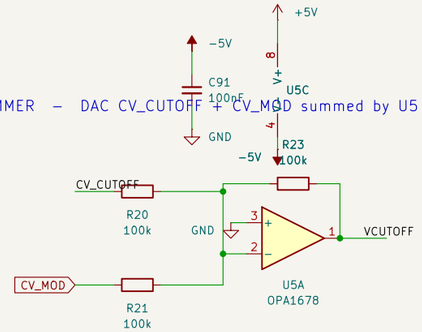
KiCad E.D.A. 10.0.6 | Id: 4/9

ANALOG FILTER / CV (stereo) – SPI in (10-pin FFC) -> DAC8565 makes CVs -> per-channel LM13700 VCF/VCA; CD4053 selects analog or FPGA-digital

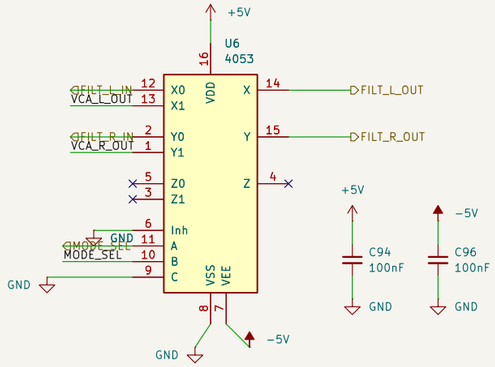
CONTROL/DAC – one 10-pin control FFC (root) feeds this DAC (CS_DAC1) + the FX DAC + MCP over ONE shared SPI bus; MODE_SEL from the expander



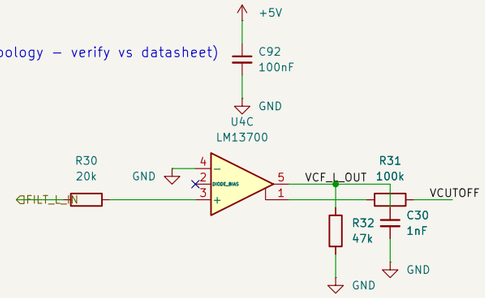
CV SUMMER – DAC CV_CUTOFF + CV_MOD summed by U5 -> VCUTOFF (drives both L and R VCFs); knob lives on the control board



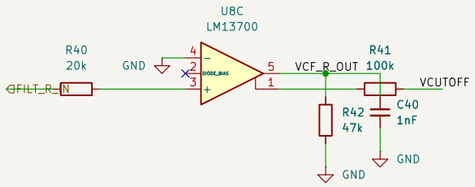
TOGGLE – CD4053: MODE_SEL selects analog (VCA_x_OUT) vs bypass (FILT_x_IN) for BOTH L and



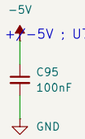
VCF+VCA L – LM13700 OTA lowpass then OTA VCA (NOTE: OTA/labc topology – verify vs datasheet)



VCF+VCA R – LM13700 OTA lowpass then OTA VCA (NOTE: OTA/labc topology – verify vs datasheet)



DECOUPLING 100nF/IC (U4/U8/U5/U6 rails +/-5V ; U7 DAC +5V)



FILT_x_IN / FILT_x_OUT are the hierarchical pins shared with the root (front-end) sheet. Power rails (+5V/-5V/GND) are global.

Sheet: /ANALOG_FILTER_CV/
File: ANALOG_FILTER_CV.kicad_sch

Title:

Size: A3 | Date: | **Rev:**
KiCad E.D.A. 10.0.6 | Id: 5/9

MASTER FILTER (stereo) — VC state-variable filter 2-pole: LP/HP/BP/notch; CV cutoff + CV resonance; mode-select mux

CHANNEL L

LPL
HPL
AUDIO_L_IN
RESFBL
R101 100k
R102 100k
R103 100k
R104 100k
R105 100k
U30A OPA1678
U30B
U30C
NOTCHL
HPL
BPL
RESFBL
C501 100nF
C502 100nF
C503 100nF
C509 100nF
R106 100k
R107 100k
R108 100k
R109 100k
R110 22k
R111 22k
R112 22k
R113 10k
R114 10k
R115 22k
R116 10k
R117 10k
R118 22k
R119 220R
R120 220R
R121 47k
R122 100k
U31A LM13700
U31C LM13700
U31D
U31E
U32C
U32D
U32E
C110 1nF
C114 1nF
C511 100nF
CV_CUTOFF
CV_RES
MODE_A
MODE_B
FILT_GND
FILT_+5V
FILT_-5V
U33 4052
AUDIO_L_OUT
C515 100nF
J15 LEFT AUDIO OUT
J17 FILTER FFC

CHANNEL R

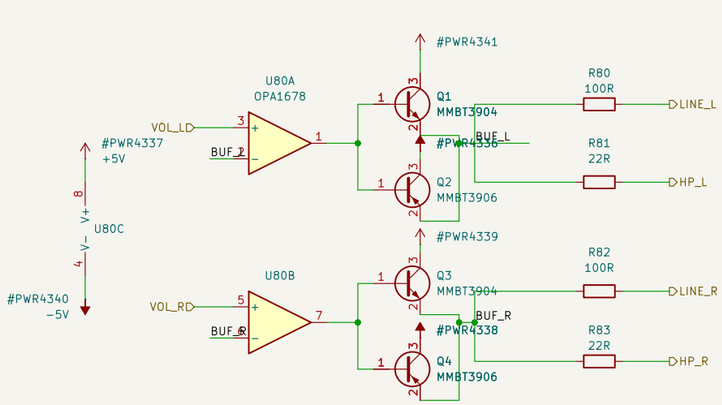
LPR
HPR
AUDIO_R_IN
RESFBR
R201 100k
R202 100k
R203 100k
R204 100k
R205 100k
U34A OPA1678
U34B
U34C
NOTCHR
HPR
BPR
RESFBR
C504 100nF
C505 100nF
C508 100nF
C510 100nF
C512 100nF
C513 100nF
R206 100k
R207 100k
R208 100k
R209 100k
R210 22k
R211 22k
R212 22k
R213 10k
R214 10k
R215 22k
R216 10k
R217 10k
R218 22k
R219 220R
R220 220R
R221 47k
R222 100k
U35A LM13700
U35C LM13700
U35D
U35E
U36C
U36D
U36E
C210 1nF
C214 1nF
CV_CUTOFF
CV_RES
MODE_A
MODE_B
FILT_GND
FILT_+5V
FILT_-5V
U37 4052
AUDIO_R_OUT
C514 100nF

DECOUPLING — 100nF at each IC's supply pins (+5V and −5V)

NOTE: OTA VC-SVF + OTA resonance VCA = prototype/verify levels, labc, buffer bias vs LM13700 datasheet before fab. ORDER_SEL reserved for the 2/4-pole cascade.

Sheet: /MASTER_FILTER/
File: MASTER_FILTER.kicad_sch
Title:
Size: A3 | Date: | Rev:
KiCad E.D.A. 10.0.6 | Id: 6/9

OUTPUT BUFFER (U80 + push-pull Q1-Q4): unity buffer w/ class-B current boost in the loop. LINE_x->1/4in(100R), HP_x->headphone(22R).



Sheet: /OUTPUT_BUF/		
File: OUTPUT_BUF.kicad_sch		
Title:		
Size: A3	Date:	**Rev:**
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FX CHORUS (true stereo) — BBD (MN3207) delay per channel, MN3101 2-phase clock swept by CV_FX3 (vibrato); wet/dry mix; bypass CD4053 on FX_EN3.

Anti-alias LPF in, reconstruction LPF out. NOTE: NO NE570 compander (not in KiCad libs) — add later for lower BBD noise. VDD=+5V (verify BBD headroom/bias + clock rate vs datasheet + real-model sim before fab).

U73A
OPA1678
VMID 3
IL_L 2
1 AA_L

U74A
OPA1678
VMID 3
OL_L 2
1 WET_L

U75A
OPA1678
GND 3
ML_L 2
1 CHW_L

VGGB
FXB_+5V
U70
MN3207
CLK1 2
CLK2 6
AA_L 3
4 VGG
5 VDD
CP1
CP2
IN
OUT1 7 BO1_L
OUT2 8 BO2_L
GND 1 FXB_GND

FXB_+5V
U72
MN3101
3 VDD
OSC1 7
OSC2 6
OSC3 5
OX1
OX2
OX3
VGG_OUT 8 VGGB
CP1 2 CLK1
CP2 4 CLK2
GND 1
FXB_GND

U73B
VMID 5
IL_R 6
7 AA_R

U74B
VMID 5
OL_R 6
7 WET_R

U75B
GND 5
ML_R 6
7 CHW_R

VGGB
FXB_+5V
U71
MN3207
CLK1 2
CLK2 6
AA_R 3
4 VGG
5 VDD
CP1
CP2
IN
OUT1 7 BO1_R
OUT2 8 BO2_R
GND 1 FXB_GND

FXB_+5V
8 V+
U73C
4 V-
FXB_-5V

FXB_+5V
8 V+
U74C
4 V-
FXB_-5V

FXB_+5V
8 V+
U75C
4 V-
FXB_-5V

FXB_+5V
U76
4053
16 VDD
CH_L_IN 12
CHW_L 13
CH_R_IN 2
CHW_R 1
X0
X1
Y0
Y1
Z0 5
Z1 3
Inh 6
A 11 FXB_d1
B 10 FX_EN3
C 9
X 14 FXB_L_OUT
Y 15 FXB_R_OUT
Z 4
VSS 8
VEE 7
FXB_GND
FXB_GND
FXB_-5V
FXB_GND

FXB_+5V
U77C
8 V+
4 V-
FXB_-5V

U77A
OPA1678
VMIDR 3
VMID 2
1 VMID
R1051 100k
VMIDR

VMIDR
R1052
100k
FXB_GND

CHW_L
R1067
22k
ML_L

FXB_R_IN
R1068
10k
IL_R

VMID
C1053
10uF
FXB_GND

R1054
47k
OSC1
OSC2

OSC3
C1055
100pF
FXB_GND

OSC2
C1056
100pF
OSC3

R1057
220k
FXB_CV1
OSC1

R1058
10k
FXB_L_IN
IL_L

R1059
10k
AA_L
IL_L

AA_L
C1060
1nF
IL_L

BO1_L
R1061
10k
OL_L

BO2_L
R1062
10k
OL_L

WET_L
R1063
10k
OL_L

WET_L
C1064
1nF
OL_L

CH_L_IN
R1065
22k
ML_L

WET_L
R1066
22k
ML_L

AA_R
R1069
10k
IL_R

AA_R
C1070
1nF
IL_R

BO1_R
R1071
10k
OL_R

BO2_R
R1072
10k
OL_R

WET_R
R1073
10k
OL_R

WET_R
C1074
1nF
OL_R

CH_R_IN
R1075
22k
ML_R

WET_R
R1076
22k
ML_R

CHW_R
R1077
22k
ML_R

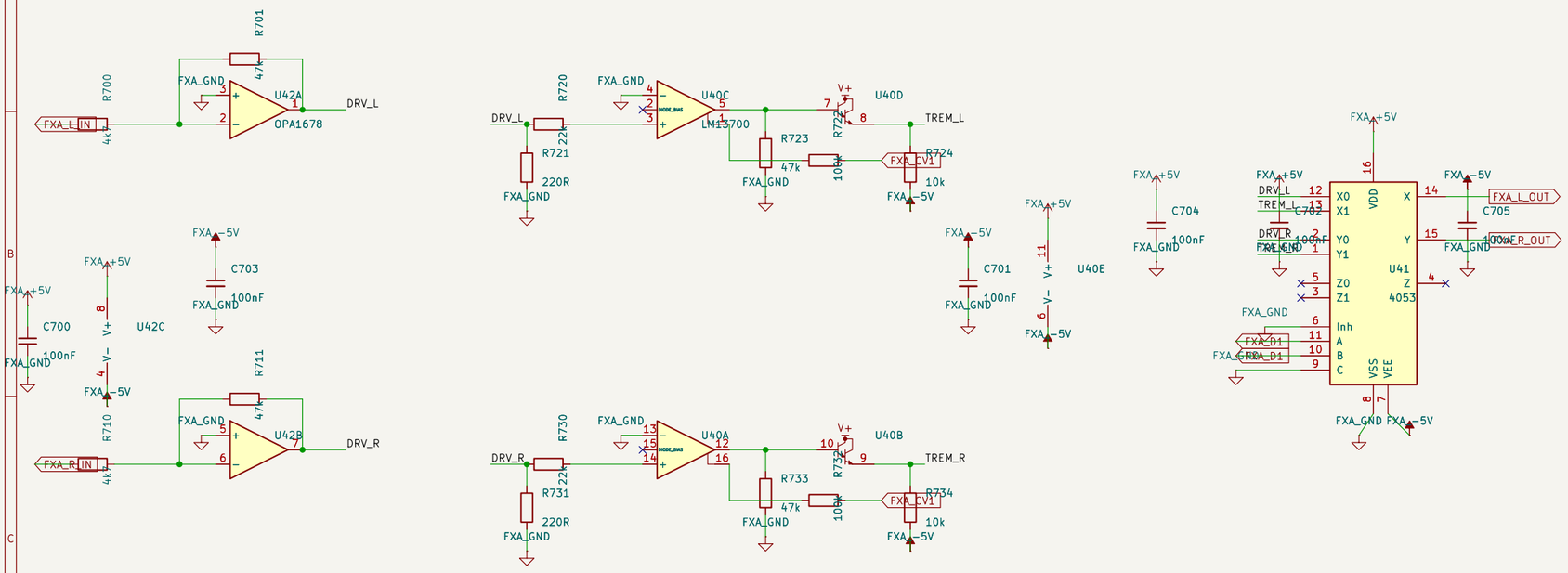
FXB_+5V FXB_-5V
DECOUPLING 100nF/IC
C1085 100nF FXB_GND
C1086 100nF FXB_GND
C1087 100nF FXB_GND
C1088 100nF FXB_GND
C1089 100nF FXB_GND
C1090 100nF FXB_GND
C1091 100nF FXB_GND
C1092 100nF FXB_GND
FXB_+5V FXB_-5V

Sheet: /FX_CHORUS/
File: FX_CHORUS.kicad_sch

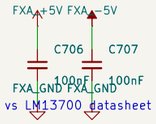
Title:

Size: A3 | Date: | **Rev:**
KiCad E.D.A. 10.0.6 | Id: 8/9

FX CHAIN – DRIVE (soft clip) + TREMOLO (OTA VCA, LFO=CV_FX1); each bypassable (FX_EN). In: FILT_x_FILT (from SVF) –> Out: FX_x_OUT (to volume)



DECOUPLING 100nF/IC



NOTE: analog FX – simulate/verify diode clip levels and OTA VCA vs LM13700 datasheet before fab.

Sheet: /FX_CHAIN/		
File: FX_CHAIN.kicad_sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. 10.0.6		Id: 9/9